REMARKS

Claims 1-26 were originally pending in this application. On June 22, 2005, Applicant responded to a restriction requirement by electing to withdraw claims 11, 12, and 20-26. Claims 1-10 and 13-19 are currently pending. The Office has rejected claims 1-10 and 13-19 under 35 USC § 103(a) as being unpatentable over Asahi (U.S. Pat. No. 6,975,516) in view of Smith et al. (U.S. Pat. No. 6,340,796; hereinafter "Smith"). Additionally, the Office has rejected claims 1-3, 5, 8, 9, 14, and 18 under USC § 103(a) as being unpatentable over Blakely (U.S. Pat. No. 6,618,266) in view of Hayashi (U.S. Pat. No. 6,809,268). This is a non-final Office action and is responsive to Applicant's communication filed on or about October 26, 2006.

Notice of Not Fully Responsive Reply

On January 9, 2007, the Office mailed a notice stating that Applicant's reply of October 26, 2006 was not fully responsive to the prior Office Action because it failed to address the rejections related to the prior art of Blakely and Hayashi. After a review of the documents in the case, page 9 of the Office Action mailed June 27, 2006 was found to be missing. Page 9 contains the rejection based on the prior art of Blakely and Hayashi. The problem was not the fault of the Patent Office. Documents from the Patent Office are received at our main office in Dayton, OH, then they are electronically scanned and sent to the person that is handling the case. During the automatic scanning process, page 9 stuck to the page 8 and was not scanned. We have implemented procedures to prevent this in the future. I thank you for your patience and the opportunity to correct our error. Please enter this reply as a replacement for the reply filed on October 26, 2006.

103(a) Rejection of Independent Claims 1 and 13 (Asahi and Smith)

Asahi does not show or suggest "an embedded discrete surface mount first decoupling capacitor mounted to the outer surface of the first reference plane layer, the first decoupling capacitor comprising a first electrode connected to the first reference plane and a second electrode connected to the second reference plane," as required by Applicant. The Office asserts that figure 8 of Asahi discloses these elements. The Office

copied figure 8 from Asahi into Appendix "A" of the Office action and added callouts not present in the figure, as disclosed by Asahi. The Office added four callouts (804-1a, 804-2a, 804-1b, and 804-2b), each pointing to a different object. Additionally, there are three other objects (804, 810, and 812) in figure 8 that are labeled by Asahi. Asahi describes these three objects (804, 810, and 812) as simply electronic components. (Col. 12, lines 8-33.) Nowhere in the description of any of the objects found in figure 8 is the term capacitor used. Furthermore, Asahi does not specifically describe the objects (804-1a, 804-2a, 804-1b, and 804-2b) labeled by the Office in Appendix "A". Absent a specific description of the objects by Asahi, it is improper for the Office to assign a description without at least providing an explanation for how it arrived at the assignment. Even if hypothetically, the objects (804-1a, 804-2a, 804-1b, and 804-2b) are the same as the labeled objects (804, 810, and 812), Asahi described them as simply electronic components. Applicant requires an embedded discrete surface mount decoupling capacitor. This element is missing from Asahi.

Applicant requires the electrodes, of each of the embedded discrete surface mount decoupling capacitors, to be attached to reference planes. A person of ordinary skill in the art would understand that the term "reference plane" refers to a power or ground plane. The Office asserts that an object 808 shown in figure 8 embodies this requirement. Applicant disagrees. Asahi describes object 808 as a "three-layered wiring board" and depicts two instances of the three-layered wiring boards 808 in figure 8. (Col. 12, line 26.) In one of the depictions, Asahi describes the lower of the three layers 802 as a "wiring pattern." (Col. 12, lines 26-27.) Asahi is silent on the function of the other two layers that make up the three-layered wiring boards 808. In Appendix "A", the Office has labeled the top layer of one the boards 808 as a "First Reference Plane Layer" and the lower layer as a "Second Reference Plane Layer." There is no support in Asahi for this assertion by the Office. The layers, in the instance of three-layered wiring board 808 that the Office has labeled, are not described or labeled by Asahi. In the other instance of the three-layered wiring board 808, the lower layer is described as a wiring pattern 802, which is not the same as a reference layer. The other layers of this instance are not labeled and there is no teaching that any of the layers are indeed reference layers. The assertion by the Office that the top and lower layers are "reference layers" is unsupported

by teachings of Asahi and therefore improper. Even if hypothetically they were reference layers, Asahi clearly shows the electrodes of the objects attached to the boards 808 are connected to each of the outer layers and the middle layer. To meet Applicants requirement that the electrodes are attached to reference planes, all three of Asahi's layers would have to be reference planes because Asahi's electrodes are connected to all three layers. This is not possible since Asahi clearly teaches that at least one of the three layers is a wiring pattern layer 802. Therefore, the Asahi fails to show or suggest at least these elements required by Applicant.

Smith teaches, "a printed wiring board structure interfaced with an integral core fabricated of a metal matrix with pitch based graphite fibers." (Col. 1, lines 8-10.) Smith fails to show or suggest the above elements missing from Asahi.

At least these elements, required by Applicant, are missing from the prior art references. Thus, the Office has failed to establish a *prima facie* case of obviousness. The rejection is improper and the claims are allowable over the prior art made of record.

103(a) Rejection of Claims 1 and 13 (Blakely and Hayashi)

The Office acknowledges Blakely does not disclose an embedded capacitor as required by Applicant and looks to Hayashi for this element. The Office asserts that "it would have been obvious to a person of ordinary skill in the art at the time of Applicant's invention to have assembly of Blakely used in the circuit board causing the capacitor to be embedded capacitors, as taught by Hayashi, in order to increase the available surface area of the board." (Office action mailed June 27, 2006, page 10.) Applicant disagrees.

Blakely teaches "decoupling capacitors must be installed together to meet the fast switching current demands of the high-speed digital circuits" and that "attempting to save space and cost by sharing vias between capacitors usually decreases each capacitor's effectiveness." (Col. 3, lines 31-35.) Blakely further states that "the present invention is a capacitor mounting pattern that allows sharing of vias yet is not subject to the inductive loss problems of the prior art." (Col. 3, lines 45-48.) Blakely's invention is clearly focused on a specific geometry for the capacitor mounting pattern which allows sharing of vias without being subject to inductive loss problems.

Hayashi teaches that when a chip capacitor is embedded in a thin prepreg adhesive layer, the layer is likely to crack in the vicinity of an electrode of the chip capacitor. The crack impairs the dielectric capability and hermetic capability of the region peripheral to the crack, which can cause the characteristics of the chip capacitor to become unstable. (See col. 1, lines 30-39.) Hayashi solves the cracking problem by the addition of inorganic filler to the resin used to embed an electronic component and by controlling the particle size of the organic filler used around the electrode of the electronic component. (See col. 1, lines 49-54.) Hayashi also depicts the chip capacitor oriented with its electrodes perpendicular to the wiring layers and shows the electrodes connected to wiring layers with vias. (See Fig. 1, elements 10, 12, 14, and 15.)

To establish a *prima facie* case of obviousness, at least the following requirements must be met: (1) the references when combined must teach or suggest all elements of the claimed subject matter; (2) there must be some motivation, suggestion or teaching to combine the referenced teachings; and (3) there must be found within the references a reasonable expectation of success. The Office Action has failed to establish a *prima facie* case of obviousness because these requirements have not been satisfied.

It is clear from the above discussion that Blakely and Hayashi are solving completely different problems in different ways. Blakely is trying to solve an inductive loss problem common with shared vias and Hayashi is trying to solve a resin cracking problem leading to a loss of hermetic seal. Hayashi's changes to the composition of the prepreg resin would provide no answers to Blakely's inductive loss with shared vias. Furthermore, Blakely's geometric mounting patterns would also not provide answers to Hayashi resin cracking problem. There is simply no motivation, suggestion or teaching to combine the references.

In fact, the layout and orientation of the capacitors used by Hayashi would not work with Blakely inventions. Blakely uses capacitors that placed horizontally on a reference layer and connected to reference layers. Hayashi uses vertically placed capacitors, mounted in a prepreg adhesive layer and connected to wiring layers with vias. Hayashi's layout, if applied to Blakely's invention, would cause Blakely's invention to fail due to the changes in geometry and the addition of extra vias. This teaches away from their combination.

There is no reasonable expectation of success to combine Blakely or Hayashi. The two references solve completely different problems in different ways. One uses a special geometry for mounting a component and the other uses the composition of a resin. As shown above, the combining of Hayashi with Blakely will cause Blakely to fail. There can be no reasonable expectation of success.

The combined references fail to show or suggest all of Applicant's claimed invention. Applicant requires an embedded capacitor that is connected to reference layers. Hayashi's embedded capacitors are connected to wiring layers not reference layers. At least this element is missing from the combined references.

The Office has failed to establish a *prima facie* case of obviousness, therefore the rejection is improper and the claims are allowable over the prior art made of record.

103(a) Rejection of the Dependent Claims

Claims depending from claims 1 and 13 are allowable for at least the same reasons presented above.

CONCLUSION

Applicant asks that the Office reconsider this application and allow all pending claims. Please charge any fees that might be due, excluding the issue fee, to deposit account 14-0225.

Respectfully submitted,

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(Electronically Filed)

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